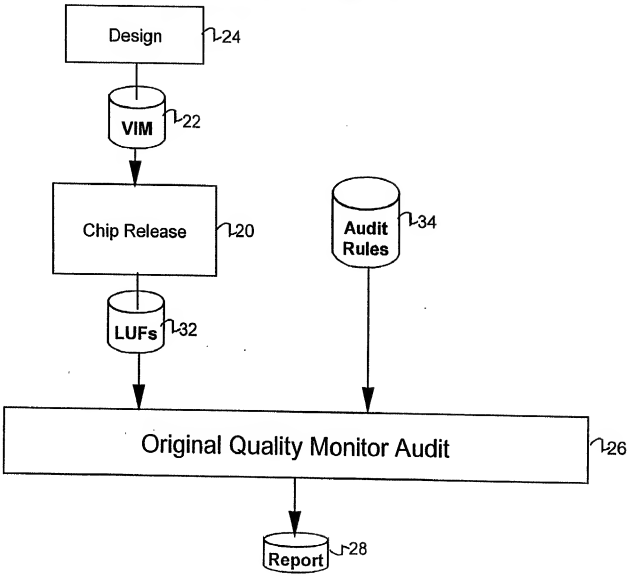

Fig. 1

```
PROGRAM Chip_Edit bin/Chip_Edit 01/04/17 09:36:02 01/04/30 15:09:36
OBJECT txplus 010111714361900
TASK Chip_Edit_net_short 0
TASK Chip_Edit_net_space 0
TASK Chip_Edit_net_loop 0
TASK Chip_Edit_net_open 0
TASK Chip_Edit_net_antenna 0
TASK Chip_Edit_net_same_intersection 0
TASK Chip_Edit_net_softpin 0
TASK Chip_Edit_net_electromigration 0
TASK Chip_Edit_net_pin_blocked 0
TASK Chip_Edit_net_same_adj 0
TASK Chip_Edit_net_wire_constraints 0
TASK Chip_Edit_place_unplaced 0
TASK Chip_Edit_place_overlap 0
TASK Chip_Edit_place_orientation 0
TASK Chip_Edit_place_bookclass 0
TASK Chip_Edit_place_bookpwrblk 0
*CHECKSUM=3112929835
```

Fig. 2

```
PROGRAM Chip_Edit Chip_Edit *
PROGRAM ElectricalRulesCheck ERCMain *
PROGRAM FillerCellCheck FCCMain *
.
.
.
TASK Chip_Edit_net_antenna 0
TASK Chip_Edit_net_electromigration 0
TASK Chip_Edit_net_loop 0
TASK Chip_Edit_net_open 0
TASK Chip_Edit_net_pin_blocked 12
TASK Chip_Edit_net_same_adj 0
TASK Chip_Edit_net_same_intersection 0
TASK Chip_Edit_net_short 0
TASK Chip_Edit_net_softpin 0
TASK Chip_Edit_net_space 0
TASK Chip_Edit_net_wire_constraints 0
TASK Chip_Edit_place_bookclass 0
TASK Chip_Edit_place_bookpwrblk 0
TASK Chip_Edit_place_orientation 0
TASK Chip_Edit_place_overlap 0
TASK Chip_Edit_place_unplaced 0
TASK ERC 0
TASK FCC 0
.
.
.
```

Fig. 3

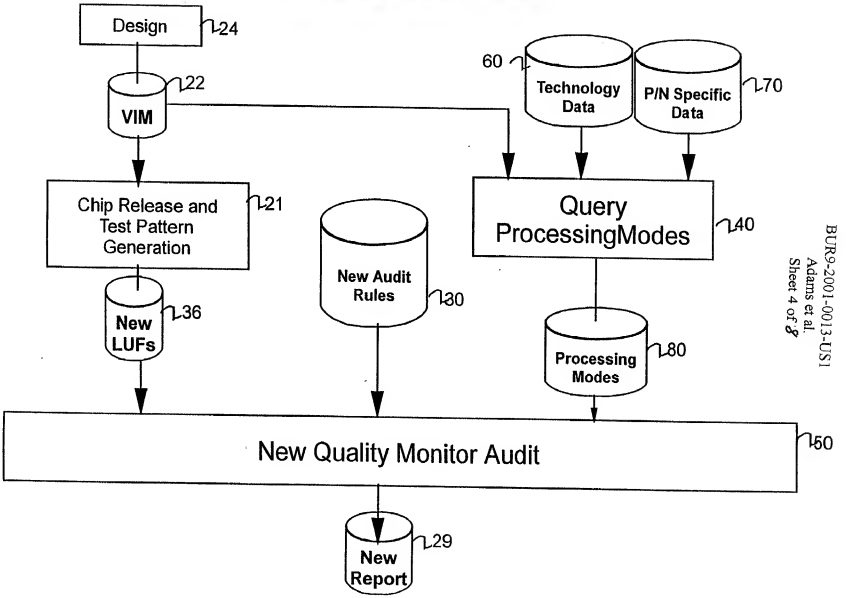

Fig. 4

```
PROGRAM TESTBENCH 0 0 0 00/05/10 20:02:39
*
OBJECT FGACHIP 010010416364000
*
OBJECT CHIP_STRUC 010010416364000
TASK MODEL_IMPORT 0
TASK CHECK_IMPORT_TIEX 0
INFO EXCLUDED_ATTRIBUTES PERF,REPOWER,PINSWAP,M062
*
OBJECT CHIP_GLOBAL
TASK CHK_ALL_MACROS_TESTED 2
INFO TEST_COVERAGE_Module_DYNAMIC 89.911095
INFO TEST_COVERAGE_Wafer_STATIC 98.637550
INFO PART_NUMBER 06K6022
*
OBJECT TESTMODE_LOGIC_ACH
TASK GEN_TSECT_LOGIC 0
TASK GEN_TSECT_LOGIC_WRP 4
TASK CHK_FLAG_OVERRIDE 0
TASK CHK_TSV_SUCCESSFUL 0
INFO BDYSCAN INT
INFO TF_PIN_ATTRIBUTE TB_LOGIC_ACH,TB_WRP_AC
INFO TDR LLCCwrp
*
OBJECT TESTMODE_IOWRAP_FCH
TASK GEN_TSECT_IOWRAP 0
TASK GEN_TSECT_IOWRAP_2xLOGn 0
TASK CHK_FLAG_OVERRIDE 0
TASK CHK_TSV_SUCCESSFUL 0
INFO BDYSCAN EXT
INFO TF_PIN_ATTRIBUTE
TB_IOWRAP_FCH,TB_IOWRAP,TB_OFLAG,TB_KFLAG
INFO TDR A6671w
```

Fig. 5

```
PROGRAM TESTBENCH 0 0 0 REQUIRED='FCH & TMD'
*
OBJECT CHIP_STRUC
TASK MODEL_IMPORT 0
TASK CHECK_IMPORT_TIEX 0
INFO EXCLUDED_ATTRIBUTES    BTV_DCS,BTV_TDS  PROHIBITED
INFO EXCLUDED_ATTRIBUTES          OPTIONAL
*
OBJECT CHIP_GLOBAL
TASK CHK_ALL_MACROS_TESTED 2
INFO TEST_COVERAGE_Wafer_STATIC >=90
INFO TEST_COVERAGE_Module_DYNAMIC >=90  REQUIRED=AC
PROHIBITED=IAC
INFO PART_NUMBER
*
OBJECT TESTMODE_LOGIC_ACH  REQUIRED=AC  PROHIBITED=IAC
TASK GEN_TSECT_LOGIC 4 OPTIONAL
TASK GEN_TSECT_LOGIC_WRP 4
TASK CHK_FLAG_OVERRIDE 0
TASK CHK_TSV_SUCCESSFUL 0
INFO BDYSCAN INT
INFO TF_PIN_ATTRIBUTE  TB_LOGIC_ACH,TB_WRP_AC
INFO TDR LLCCwrp
*
OBJECT TESTMODE_IOWRAP_FCH
TASK GEN_TSECT_IOWRAP 4
TASK GEN_TSECT_IOWRAP_2xLOGn 4  OPTIONAL
TASK CHK_FLAG_OVERRIDE 0
TASK CHK_TSV_SUCCESSFUL 0
INFO BDYSCAN INT PROHIBITED
INFO BDYSCAN EXT
INFO TF_PIN_ATTRIBUTE TB_IOWRAP_FCH,TB_IOWRAP,TB_OFLAG,TB_KFLAG
INFO TDR A6671w
```

Fig. 6

Record type	REQUIRED	OPTIONAL	PROHIBITED
PROGRAM	This PROGRAM must be present in the LUF and all OBJECT, TASK and INFO records for this PROGRAM are processed. All of these records whose own conditions are true must "pass".	If this PROGRAM is present in the LUF, all OBJECT, TASK and INFO records for this PROGRAM are processed. All of these records whose own conditions are true must "pass".	If this PROGRAM is present in the LUF, a failing error message is written.
OBJECT	This OBJECT must be present in the LUF for the PROGRAM, and all TASK and INFO records for this OBJECT are processed. All of these records whose own conditions are true must "pass".	If this OBJECT is present in the LUF for the PROGRAM, all TASK and INFO records for this OBJECT are processed. All of these records whose own conditions are true must "pass".	If this OBJECT is present in the LUF for the PROGRAM, a failing error message is written.
TASK	This TASK must be present in the LUF for the OBJECT and PROGRAM, with a return code less than or equal to the maximum specified code.	If this TASK is present in the LUF for the OBJECT and PROGRAM, its return code must be less than or equal to the maximum specified code.	If this TASK is present in the LUF for the OBJECT and PROGRAM, a failing error message is written, regardless of whether the completion code is <= the max allowed value.
INFO	This INFO must be present in the LUF for the OBJECT and PROGRAM, and the value in the LUF must match the value in the audit rule.	If this INFO is present in the LUF for the OBJECT and PROGRAM, a numeric value in audit rule must match the numeric value in the LUF. If there is no value in the audit rule, there are no error messages. In the case of a character value in the audit rule, there is no message if that value is present or missing in the LUF.	If this INFO is present in the LUF for the OBJECT and PROGRAM, and no value or a numeric value is given on the INFO, a failing message is written regardless of whether the value matches or not. If a character value is given on the INFO, the error message is only written if the value matches as well as the name.

Fig. 7

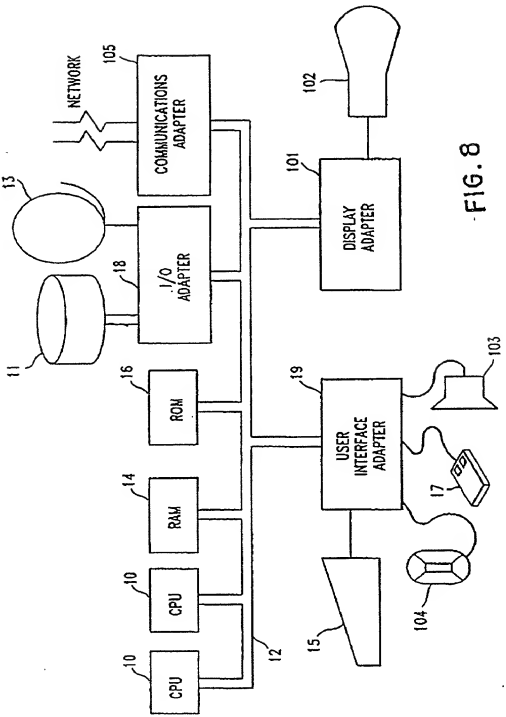
NETWORK
105
COMMUNICATIONS ADAPTER
102
13
101
DISPLAY ADAPTER
18
I/O ADAPTER
11
16
ROM
19
USER INTERFACE ADAPTER
103
14
RAM
17
10
CPU
104
10
CPU
12
15

FIG. 8